RANDOM ACCESS MEMORY WITH DATA STROBE LOCKING CIRCUIT

Abstract

A random access memory comprises a latching circuit configured to receive a first signal and provide a second signal corresponding to the first signal to latch data signals into the random access memory. The random access memory comprises a logic circuit configured to provide a first response after a predetermined number of the data signals have been latched into the random access memory by the second signal. The latching circuit is configured to receive the first response and lock the second signal to a logic level based on the first signal and the first response to prevent inadvertent latching of other data signals.